ESD1024c – Configurable 1024/512 point FFT

Introduction

The ESD1024p core implements *1024 or 512 point FFT* in hardware. It can be dynamically configured to process one 1024 or two simultaneous 512 point FFT/IFFT operation.

Applications

- WIMAX
- Communication system
- OFDM
- UWB

Features

- Supports 512 and 1024-point FFT and IFFT and can switch dynamically
- Can process up-to two 512 FFT simultaneously (well suited for MIMO application)
- Built-in bit reversal. Outputs in Natural order
- Supports reading output data in any order (read address)
- Low Latency. Can be customized to improve latency vs. gate count
- Throughput of 1 sample per clock
- Parameterized bit widths and fixed-point option.
- Test bench with fixed-point Matlab model
- Available in ASIC and FPGA technologies
- Minimal gate count implementation
- Supports flushing and re-starting the FFT instantly.
- Configurable bit width based on SQNR requirement for random inputs or for a specific stimuli pattern.
- Customization for OFDM applications

Pin Description

Name	I/O	Width	Description
clk	1	In	Clock
rst_n	1	In	Active low asynchronous reset
clr	1	In	Active high Synchronous Reset
fft_mode	1	In	0 : FFT operation 1 : IFFT operation
num_pts mode	2	Input	0 →1024 point FFT/IFFT operation 1 → 1 512 point FFT/IFFT operation 2 → 2 512 point FFT/IFFT operation 3 → Reserved
din_i	N	In	N bit in-phase input data
din_q	N	In	N bit quad-phase input data
din_vld	1	In	Input Data Valid.
fft_din_start	1	In	Start the FFT computation. This signal should be asserted either on the last input data sample or anytime after sending all input data. Internal FFT engine will start FFT computation when fft_din_start is sampled high on the clock edge. FFT output will be available after fixed latency.
in_addr_mode	1	In	Input Address mode. 1'b0 → Use internal addressing to store input data into the internal buffers. 1'b1 → Use external addressing (din_addr) to store input data into the internal buffers.
din_addr	10	In	Input address when in_addr_mode is set to 1.
out_addr_mode	1	In	Output Address mode. 1'b0 → Use internal addressing to read the FFT output data from the internal buffers. 1'b1 → Use external addressing (dout_addr) to read the FFT output data from internal buffers.
dout_addr	10	In	Output address when out_addr_mode is set to 1. In FFT 512 mode, dout_addr[9] is ignored.
fft_dout_i	N	Out	N bit in-phase output data
fft_dout_q	N	Out	N bit quad-phase output data
fft_dout_vld	1	Out	Output data valid
fft_dout_start	1	Out	Asserted on the first output point of FFT. This signal is asserted after fixed latency from fft_din_start.

Functional Description

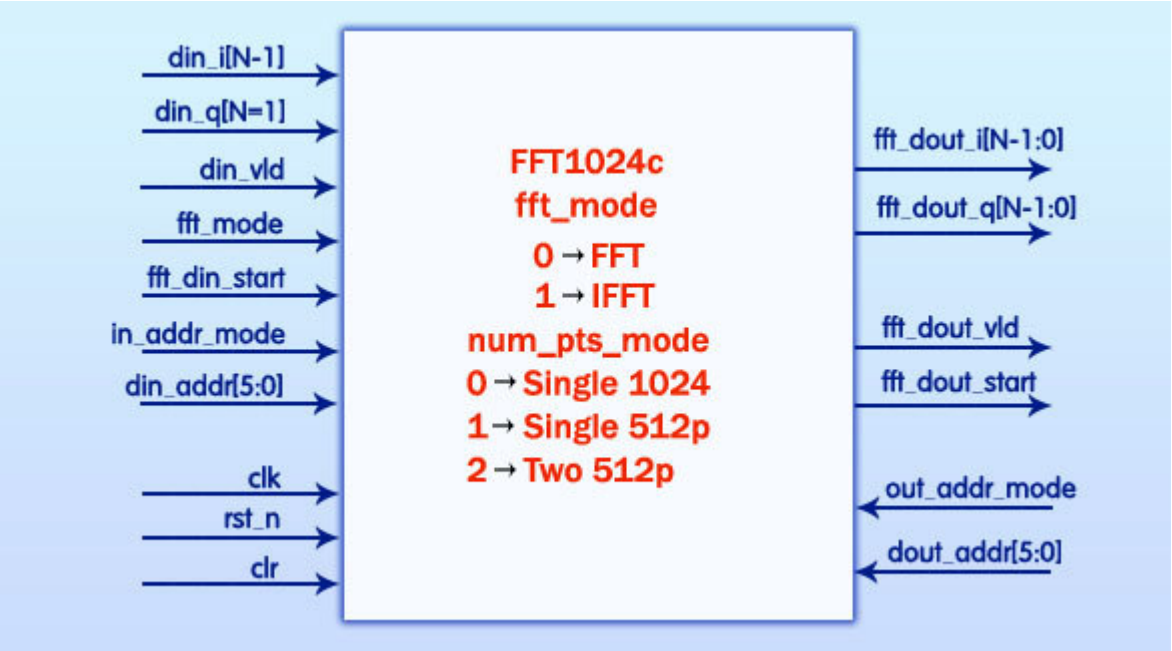

Figure 1. ESD1024c Timing Diagram

ESD1024c can process single stream of 1024 pt FFT/IFFT or 2 streams of 512 pt FFT/IFFT simultaneously.

ESD1024c supports two different modes of input data/output data streaming.

a. Natural order: In natural order the input buffer addressing is controlled internally. On reset the internal address is set to 0 corresponding to the first fft/ifft input point.

b. In external address mode, (in_addr_mode ==1), the input data is stored inside internal buffer at the location indicated by din_addr.

The FFT or IFFT radix operations start when fft_din_start pulse is sampled high. The FFT data output will be streamed out after fixed latency. The fft_dout_start pulse is asserted on the first output data sample.

Similar to input address mode, output address mode can also be controlled internally or externally by providing dout_addr.

Interface timing Diagram

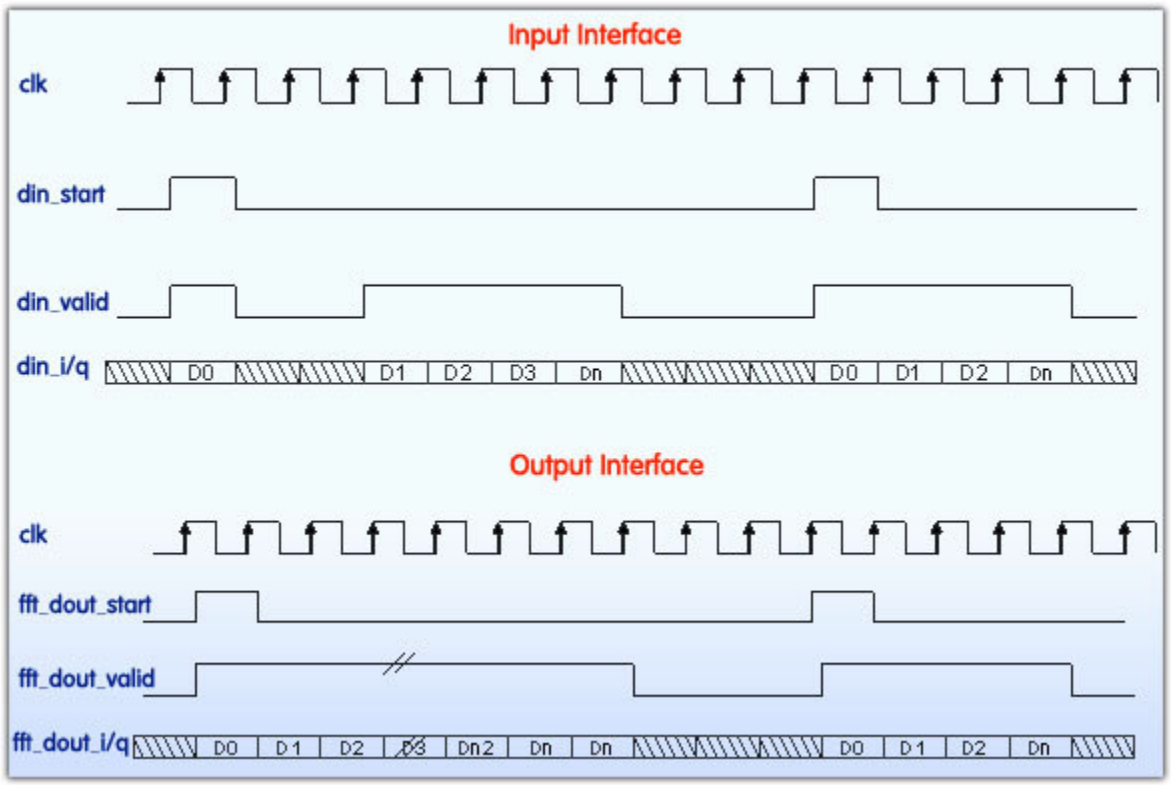

Figure 2. ESD1024c Timing Diagram

Deliverables

- Synthesizable Verilog RTL source code
- Fixed-point matlab model.
- Simulation scripts
- Self-checking Test environment
  - Test-bench
  - Test-vectors
  - Expected results
- Synthesis scripts
- User Documentation

Sales Representatives

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