ESD0064 – 64 POINT FFT

Introduction

The ESD0064 core implements 64 point FFT in hardware. FFT 64 works on blocks of 64 complex data samples.

Applications

- IEEE802.11 Wi-Fi
- GPS
- Communication system

Features

- Supports both FFT and IFFT
- In built bit reversal algorithm
- Low Latency
- Throughput of 1 sample per clock
- Parameterized bit widths and fixed point option.
- Test bench with fixed point Matlab model
- Matlab model can be used to tune the bit-width to get the SQNR performance.
- Available in ASIC and FPGA technologies
- Minimal gate count implementation
- Supports flushing and re-starting the FFT operation instantly

Pin Description

Name	I/O	Width	Description
clk	1	In	Clock
rst_n	1	In	Active low asynchronous reset
clr	1	In	Active high Synchronous Reset
fft_mode	1	In	0 : FFT operation 1 : IFFT operation
din_i	N	In	N bit in-phase input data
din_q	N	In	N bit quad-phase input data
din_vld	1	In	Input Data Valid.
fft_din_start	1	In	Start the FFT computation. This signal should be asserted either on the last input data sample or anytime after sending all input data. Internal FFT engine will start FFT computation when fft_din_start is sampled high on the clock edge. FFT output will be available after fixed latency.
in_addr_mode	1	In	Input Address mode. 1'b0 → Use internal addressing to store input data into the internal buffers. 1'b1 → Use external addressing (din_addr) to store input data into the internal buffers.
din_addr	6	In	Input address when in_addr_mode is set to 1.
out_addr_mode	1	In	Output Address mode. 1'b0 → Use internal addressing to read the FFT output data from the internal buffers. 1'b1 → Use external addressing (dout_addr) to read the FFT output data from internal buffers.
dout_addr	6	In	Output address when out_addr_mode is set to 1.
fft_dout_i	N	Out	N bit in-phase output data
fft_dout_q	N	Out	N bit quad-phase output data
fft_dout_vld	1	Out	Output data valid
fft_dout_start	1	Out	Asserted on the first output point of FFT. This signal is asserted after fixed latency from fft_din_start.

Functional Description

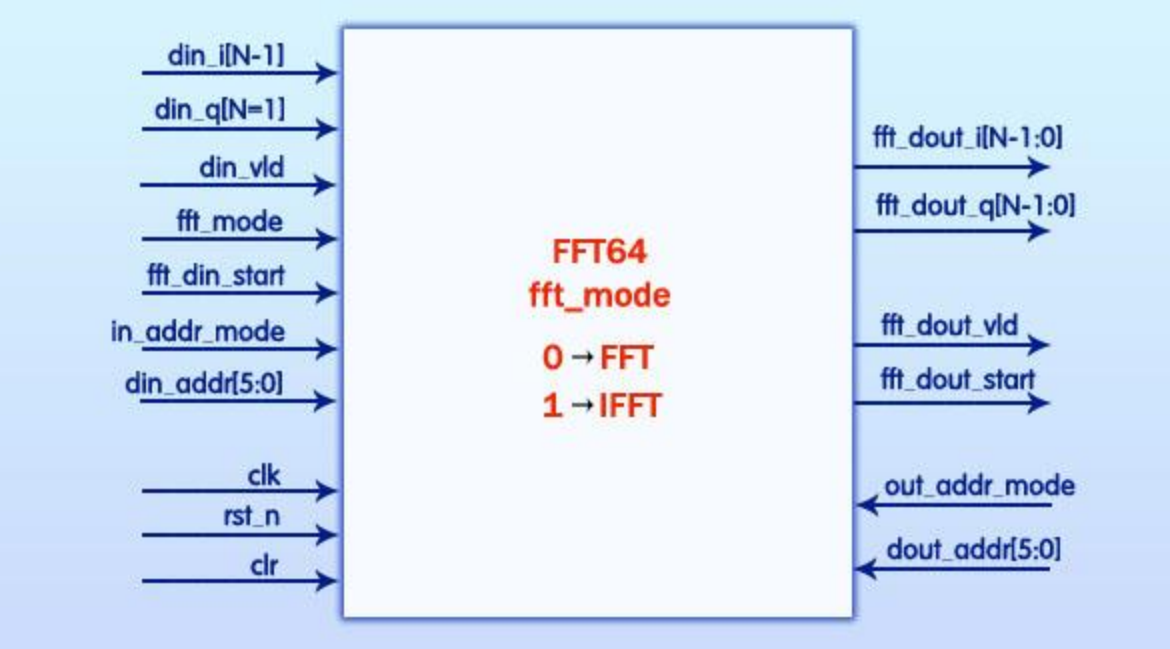

Figure 1. ESD0064 Block Diagram

ESD0064 can process 64 pt FFT or 64 pt IFFT based on input mode (fft_mode). The mode can be switched dynamically.

ESD0064 supports two different modes of input data/output data streaming.

a. Natural order: In natural order the input buffer addressing is controlled internally. On reset the internal address is set to 0 corresponding to the first fft/ifft input point.

b. In external address mode, (in_addr_mode ==1), the input data is stored inside internal buffer at the location indicated by din_addr.

The FFT or IFFT radix operations start when fft_din_start pulse is sampled high. The FFT data output will be streamed out after fixed latency. The fft_dout_start pulse is asserted on the first output data sample.

Similar to input address mode, output address mode can also be controlled internally or externally by providing

Interface timing Diagram

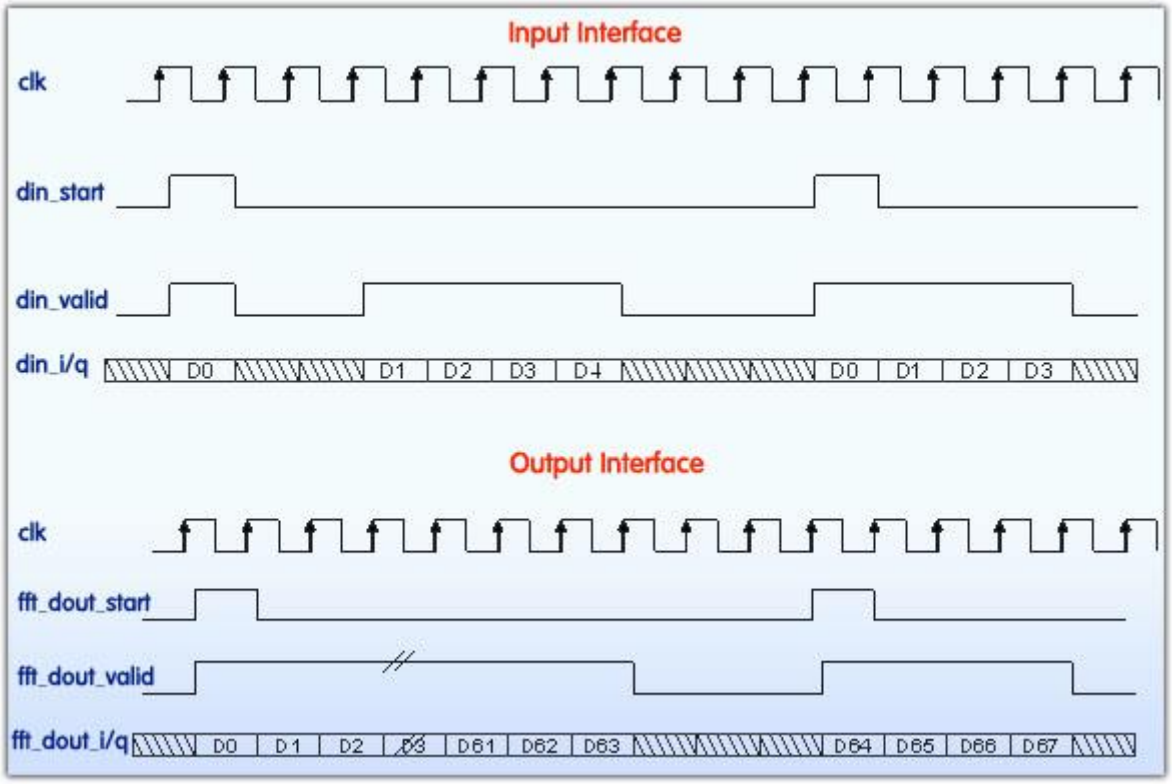

Figure 2. ESD0064 Timing Diagram

Deliverables

- Synthesizable Verilog RTL source code
- Fixed-point matlab model.
- Simulation scripts
- User Documentation
- Self-checking Test environment
  - Test-bench
  - Test-vectors
  - Expected results
- Synthesis scripts
- User Documentation

Sales Representatives

For pricing information:

Esencia Technologies Inc.
2041 Mission College Blvd Suite 100
Santa Clara, CA 95054
Tel: (408) 736-8284
Web: www.esenciatech.com
E-mail: sales@esenciatech.com

About Esencia

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