ES7010 - EScalaOne Design Platform
Product Brief

Introduction

EScala is a fully configurable CPU soft-core generator. Configuration can be user or application driven (semi-automated). EScala targets low power deeply embedded applications with high performance and bandwidth requirements, conventionally reserved to fixed function logic.

Features

- 32-bit VLIW with configurable number of issue slots (1-32)
- Harvard architecture with tightly coupled memories
- Configurable number of load/store units (1-32)
- Configurable number of input/output channels accessible from any slot
- Data-flow architecture with simple programming model
- Baseline RISC-like instruction set derived from OpenRISC architecture
- Number of registers tunable to application needs
- Common register file accessible from all slots

Optional Features

- User defined Extension Instructions that augment the basic instruction set
- In System Debug module accessible through JTAG port
- Dual/Quad SIMD instructions
- Programmable Interrupt controller
- Program Memory Compression
- Application specific extension instruction libraries, targeting:
  - Audio
  - Video
  - Signal processing
  - Baseband processing
- Programmable address generation units

Applications

- High bandwidth data intensive algorithms
- Replacement for fixed function high-performance blocks, where programmability is a plus
- Low power / low gate count system controllers
- Rapid Algorithm FPGA prototyping
- High frequency trading FPGA applications
- Low latency computing applications
- Complex control applications

Tools

- OpenRISC gnu compiler / assembler / debugger
- EScala's Instruction Set Simulator
- EScala's CustomFIT compiler back-end
  - Advanced VLIW instruction scheduling
  - Instruction set analysis / customization
  - Automated complex instruction generation
  - Instruction encoding optimization
  - Configuration Parameter Scanning
  - Miscellaneous optimization steps

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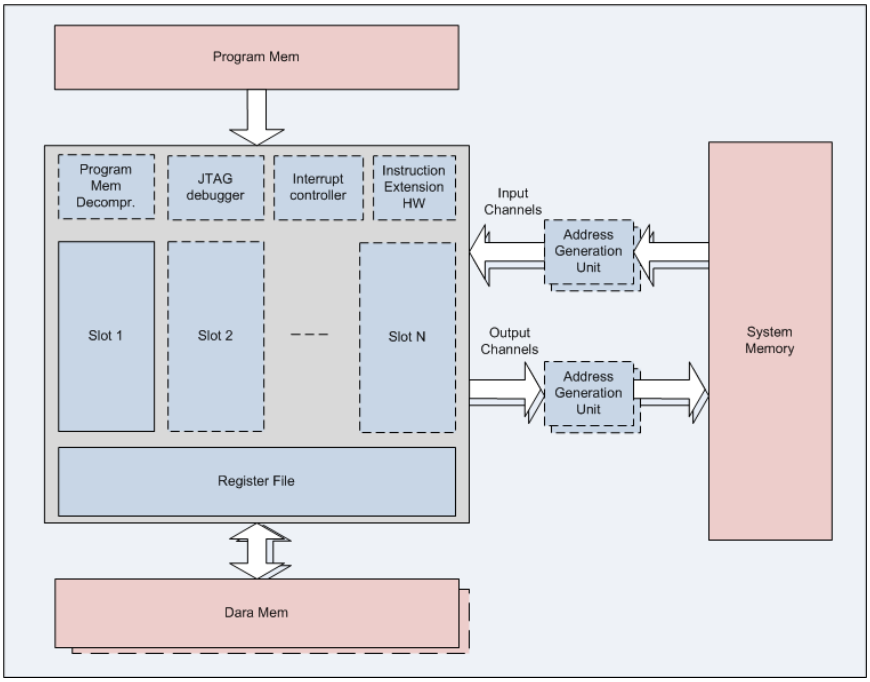
Top-Level Diagram



Deliverables

- Synthesizable Verilog RTL source
- Simulation scripts
- Self-checking Test environment
  - Test-bench
  - Sanity regression
- Synthesis scripts
- User Documentation
- Complete SW toolset for Linux
  - Gnu compiler/assembler/linker
  - CustomFIT SW
  - EScala Instruction Set Simulator

Sales Representatives

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About Esencia

Esencia Technologies Inc. provides IP cores and design services for the semiconductor industry. We can assist the core generation process to build the best fitting core for your application.