

## Introduction

The ES 0100-5 implements Viterbi Algorithm for 802.11 standard convolution code polynomials with trace back depth equal to 40. This core implementation is optimized for one symbol (2-bits) per 5 clocks throughput rate. The latency of the first output is 41 input symbols plus 45 clocks. The last 5 bytes are flushed out with a latency of 40 clocks after receiving the last input. A 40 bit output is also available to get the entire 40 bits. If the burst size is smaller than 40 bits, the output latency is equal to the size of the burst.

## Applications

- 802.11 standard

## Features

- ❖ Supports 802.11 a/b/g standards.
- ❖ Low gate count implementation
- ❖ Simple external interface
- ❖ Additional output ports to access all the flush bits in one clock to reduce latency on 802.11 phy header.
- ❖ Option to optimize on flush latency with additional hardware.
- ❖ Low Power
- ❖ Available in ASIC and FPGA Technologies.

## Pin Description

Name	I/O	Width	Description
clk	Input	1	System Clock input
reset	Input	1	Asynchronous active low reset
din	Input	2	input data (dibits)
din_valid	Input	1	validates din if busy is low
din_first	Input	1	indicates the first bit of block. (optional)
din_last	Input	1	indicates the last bit of the block
vit	Output	7.0	8 bit viterbi decoded output
vit_vld	Output	1	validates output
vit_busy	Output	1	when asserted inputs on din and din_vld are ignored
vit_flush_data	Output	40	when asserted inputs on din and din_vld are ignored

Table 1. ES0100-5-Viterbi Decoder interface.

## Functional Description

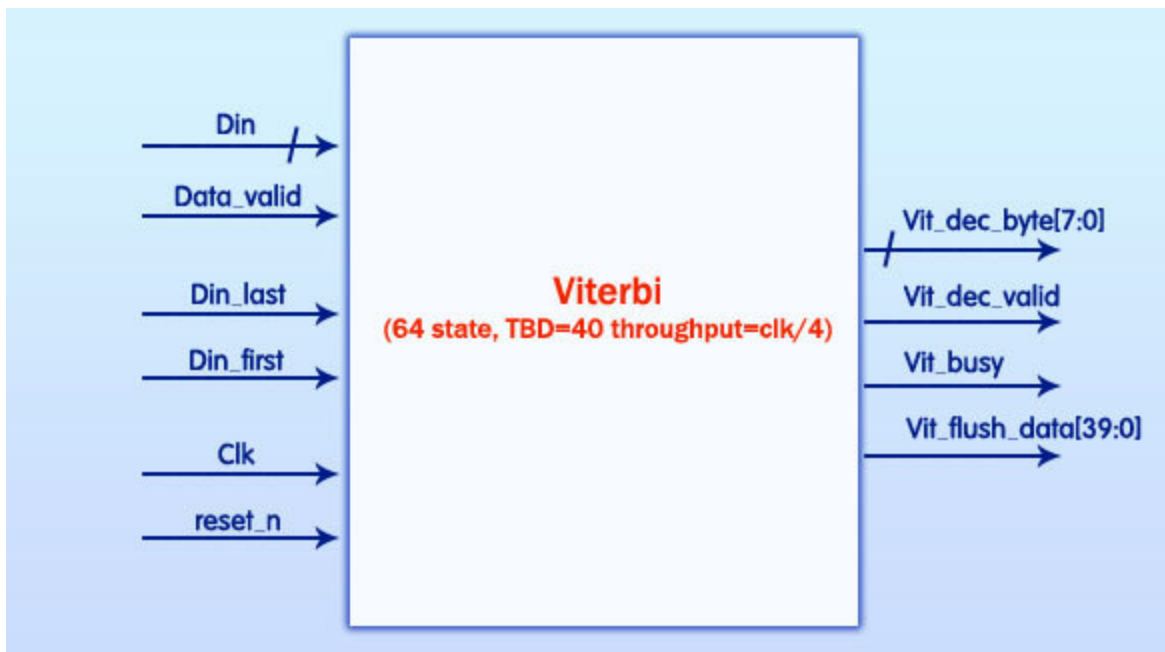


Figure 1. ES0100-5

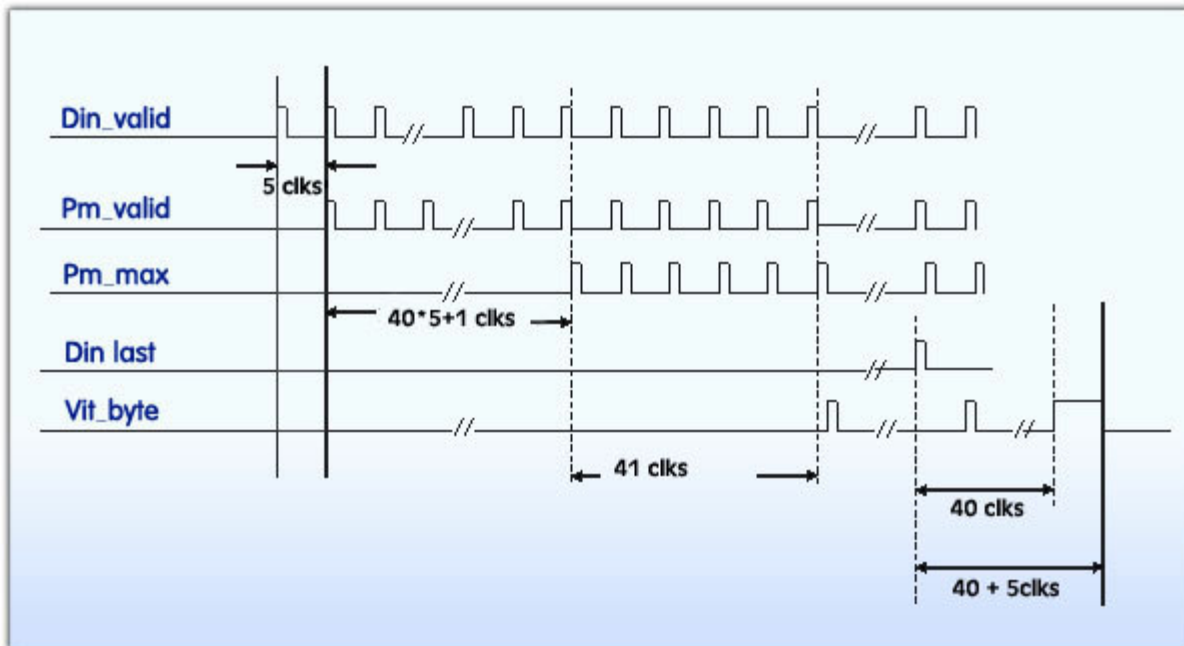


Figure 2. ES0100-5 Interface Timing Diagram

## Deliverables

- ❖ Synthesizable Verilog RTL source code
- ❖ Fixed Point Matlab Model
- ❖ Simulation scripts
- ❖ Self-checking Test environment
  - Test-bench
  - Test-vectors
  - Expected results
- ❖ Synthesis scripts
- ❖ User Documentation

**Sales Representatives**

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