ESD0064 – 64 POINT FFT datasheet

1 Introduction

The ESD0064 core implements *64 point FFT* in hardware. FFT 64 works on blocks of 64 complex data samples.

2 Features

- Supports both FFT and IFFT
- In built bit reversal algorithm
- Low Latency
- Throughput of 1 sample per clock
- Parameterized bit widths and fixed point option.
- Test bench with fixed point Matlab model
- Matlab model can be used to tune the bitwidth to get the SQNR performance.
- Available in ASIC and FPGA technologies
- Minimal gate count implementation
- Supports flushing and re-starting the fft instantly

3 Top level block diagram

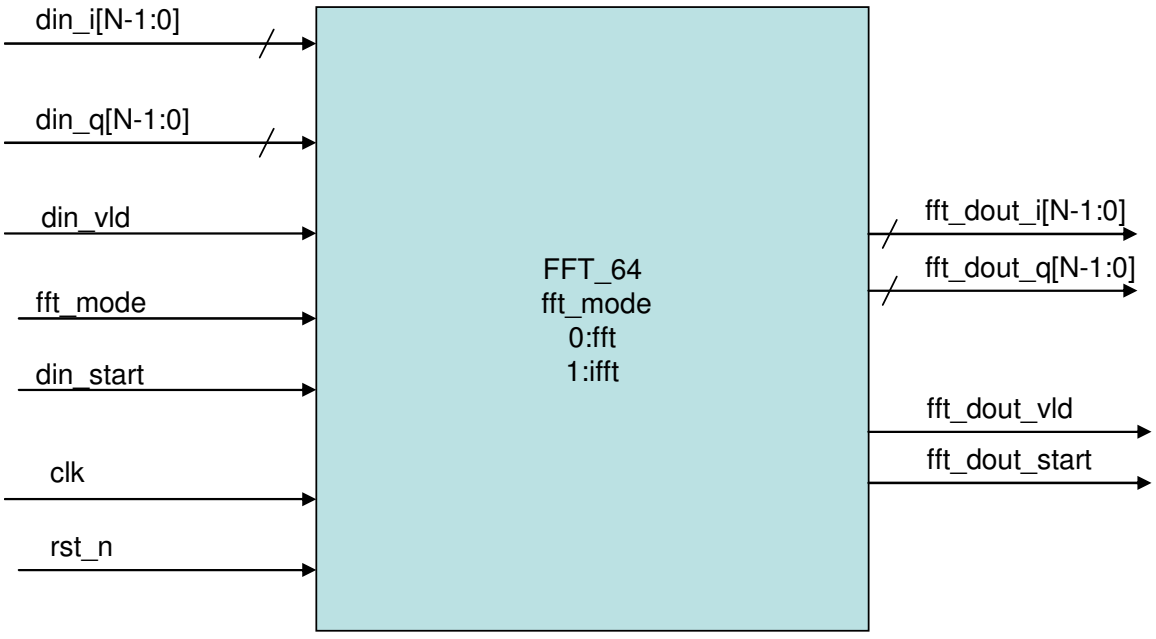


Figure1. Top level block diagram

4 Interface

Signal	Width	Direction	Description
clk	1	In	Positive edge clock
rst_n	1	In	Active low asynchronous reset
din_i	N	In	N bit in-phase input data
din_q	N	In	N bit quad-phase input data
din_vld	1	In	when asserted data on din_i and din_q are valid
din_start	1	In	re-start the fft computation. If din_vld is also asserted on the same clk, the current data is used as the first data. din_start is provided to flush if any residue data is present in the fft memories. If back to back fft data are provided, it is not required to toggle din_start at the beginning of every fft.
fft_mode	1	In	0: fft 1: ifft
fft_dout_i	N	Out	N bit in-phase output data
fft_dout_q	N	Out	N bit quad-phase output data
fft_dout_vld	1	Out	Output data valid
fft_dout_start	1	Out	Asserted on the first output point of fft

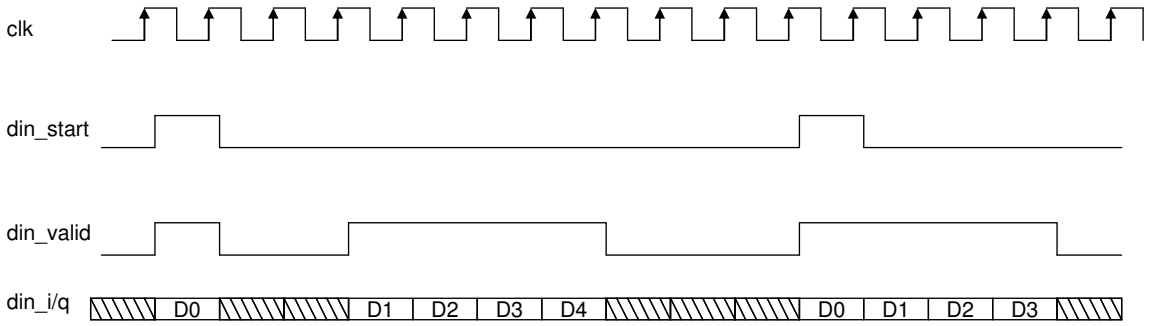
5 Theory of operation

The core has two modes of operation: FFT and IFFT.

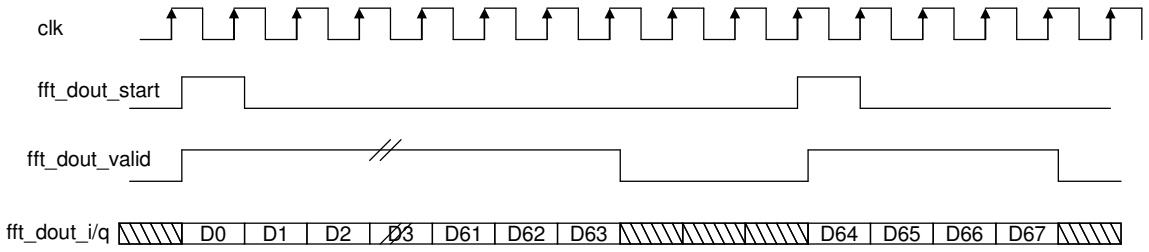
5.1 Interface timing Diagram

The following figure shows the interface timing diagram of ESD0064.

Input interface

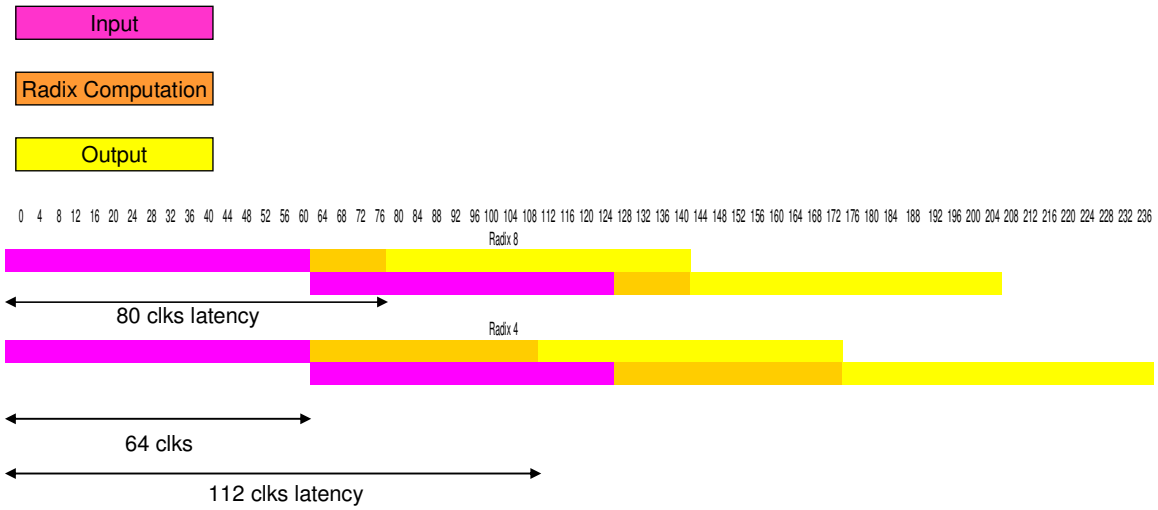


Output Interface



Note:
The input data din can be continuous or stalled. The din_valid can be asserted continuously. The output data is always in bursts of 64.

5.2 Latency diagram



6 Implementation Choices

Following Table describes the latency and gate count trade off of 3 different implementations.

R4 : Single Radix-4 hardware
2R4: Two Radix-4 Hardware
R8 : One Radix-8 Hardware

Assumption bit width after bit growth N = 10

FFT	64	Bit Width	10
	R4	2R4	R8
Memory bits	2560	2560	2560
mem conf	2X4x16dX20w	2X8x8dX20w	2X8x8dX20w
mem gates (4.5 per bit)	10240	11240	11240
Latency	112	88	80
Complex multipliers	4	8	8
mult gates	12000	24000	24000
complex adders	4	8	8
adder gates	800	1600	1600
Addr gen + mux	2000	4000	4000
Total Gate Count	25040	40840	40840